IN THE CLAIMS

1. (Currently amended) A voltage boosting circuit comprising:

boosting capacitors that include a first boosting capacitor connected to a driving node and a last boosting capacitor configured to output a boosting voltage; ~~and~~

switches configured to connect the boosting capacitors in series in response to a control signal, the boosting voltage configured to vary as a voltage level at the driving node changes according to a logic state of a boosting level control signal; and

a logic device having an output applied to the driving node and an input to receive the boosting level control signal, wherein the control signal and the boosting level control signal are configured to operate independently of each other.

2. (Original) The voltage boosting circuit of claim 1, configured such that when the boosting level control signal is in a first logic state, the voltage level at the driving node changes from a ground voltage level to an external supply voltage level, thus increasing the boosting voltage level.

3. (Previously presented) The voltage boosting circuit of claim 2, configured such that when the boosting level control signal is in a second logic state, the voltage level at the driving node is fixed at a ground voltage level, thus decreasing the boosting voltage level.

4. (Original) The voltage boosting circuit of claim 1, wherein the logic state of the boosting level control signal is configured to enter a logic high state or a logic low state in response to an external supply voltage level.

5. (Original) The voltage boosting circuit of claim 4, further comprising an external supply voltage detector configured to detect the external supply voltage level and to generate the boosting level control signal.

6. (Currently amended) A method of generating a boosting voltage in a voltage boosting circuit that includes boosting capacitors with a first boosting capacitor connected to a driving node and a last boosting capacitor that outputs the boosting voltage, ~~and~~ switches that connect the boosting capacitors in series in response to a control signal, and a logic

device having an output applied to the driving node and an input to receive a boosting level control signal, the method comprising:

increasing the boosting voltage by changing a voltage level at the driving node from a ground voltage level to an external supply voltage level when the [[a]]boosting level control signal is in a first logic state; and

decreasing the boosting voltage by an amount approximately equal to the external supply voltage level by fixing the voltage level at the driving node to the ground voltage level when the boosting level control signal is in a second logic state, wherein the control signal and the boosting level control signal are configured to operate independently of each other.

7. (Original) The method of claim 6, further comprising:

detecting the external supply voltage level and changing the boosting level control signal to the first logic state when the external supply voltage level is less than a reference voltage level; and

detecting the external supply voltage level and changing the boosting level control signal to the second logic state when the external supply voltage level is greater than the reference voltage level.

8. (Previously presented) The voltage boosting circuit of claim 1, wherein the driving node is configured to have a constant voltage during both an open and closed state of the switches.

9. (Previously presented) The voltage boosting circuit of claim 3, having N boosting capacitors, wherein N is an integer greater than 1.

10. (Previously presented) The voltage boosting circuit of claim 9, wherein the boosting level voltage is substantially equal to (N+1) multiplied by the external supply voltage level for the first logic state, and substantially equal to N multiplied by the external supply voltage level for the second logic state.

11. (Previously presented) The voltage boosting circuit of claim 1, wherein the first boosting capacitor is connected to a NOR gate.

12. (Previously presented) The voltage boosting circuit of claim 1, wherein the voltage level at the driving node is responsive to an input signal that is logically combined with the boosting level control signal.

13. (New) The voltage boosting circuit of claim 1, further comprising an external supply voltage detector to detect an external supply voltage, wherein the external supply voltage detector outputs a logic signal responsive to the external supply voltage.

14. (New) The voltage boosting circuit of claim 13, wherein the external supply voltage detector output is the boosting level control signal.

15. (New) A voltage boosting circuit, comprising:

a first boosting capacitor and a second boosting capacitor, wherein the second boosting capacitor outputs a boosted voltage;

one or more switches, which are responsive to a first control signal, to connect the first and the second boosting capacitors in series;

a pull-up transistor circuit and a pull-down transistor circuit, both pull-up and pull-down transistor circuits each having transistors that are connected to the one or more switches; and

a logic device, which is responsive to a second control signal, for applying one of a plurality of voltage levels to the first boosting capacitor, wherein the second control signal and the first control signal are configured to operate independently of each other.

16. (New) The voltage boosting circuit of claim 15, further comprising one or more additional boosting capacitors between the first and the second boosting capacitors.

17. (New) The voltage boosting circuit of claim 16, further comprising one or more additional switches to connect the one or more additional boosting capacitors and the first and the second boosting capacitors in series in response to the first control signal.

18. (New) The voltage boosting circuit of claim 15, further comprising a precharge control signal commonly connected to both the pull-up transistor circuit and the pull-down transistor circuit.

19. (New) The voltage boosting circuit of claim 15, wherein the pull-up transistor circuit and the pull-down transistor circuit are both commonly responsive to a precharge control signal.

20. (New) The voltage boosting circuit of claim 15, wherein the logic device includes a NAND gate.

21. (New) The voltage boosting circuit of claim 1, further comprising a transistor disposed between one side of the first boosting capacitor and an external power supply for affecting the voltage at the first boosting capacitor depending on the driving state of the transistor.